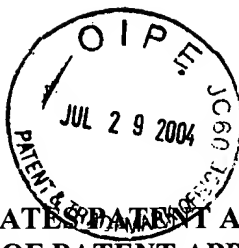


Docket No.: 50432-022 (F0379)



AF/2811 ZFW

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Application of : Customer Number: 20277
Lu YU, et al. : Confirmation Number: 5047
Application No.: 09/785,445 : Group Art Unit: 2811
Filed: February 20, 2001 : Examiner: H. K. Vu
For: SINGLE DAMASCENE INTEGRATION SCHEME FOR PREVENTING COPPER
CONTAMINATION OF DIELECTRIC LAYER

REPLY TO NOTIFICATION OF NON-COMPLIANCE WITH 37 CFR 1.192(c)

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Notification of Non-Compliance With 37 CFR 1.192 mailed July 1, 2004. and further to the Appeal Brief filed on April 9, 2004 in support of the Notice of Appeal filed February 27, 2004. Submitted herewith in triplicate is Appellants' revised Appeal Brief. Please note the Appeal Brief fee has already been charged to Deposit Account 500417 on April 12, 2004 (Control No. 93).

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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REVISED APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed February 27, 2004, and in response to the Notice of Non-Compliance dated July 1, 2004.

I. **REAL PARTY IN INTEREST**

The real party in interest is Advanced Micro Devices, Inc.

II. **RELATED APPEALS AND INTERFERENCES**

Appellants are unaware of any related appeals and interferences.

III. STATUS OF CLAIMS

Claims 2, 5-6, and 14-18 have been cancelled. Claims 1, 3-4, 7-13, and 19-30 are pending in this application. Of those claims, claims 3-4 have been finally rejected, claims 1 and 7-13 have been allowed and claims 19-30 have been withdrawn. It is from the final rejection of claims 3 and 4 that this Appeal is taken.

IV. STATUS OF AMENDMENTS

No amendment to the claims has been filed subsequent to the Final Office Action dated December 1, 2003.

V. SUMMARY OF INVENTION

The present invention addresses and solves the problem of contamination of silicon oxide and silicon from materials such as copper in a semiconductor device (page 5 of Appellants' disclosure, lines 13-14). Diffused copper decreases the dielectric strength of these materials, thereby increasing their conductivity, and this results in short circuits and device failure (page 5, lines 14-20). Copper contamination occurs when corners 18 of vias 16 are rounded using a reverse physical sputtering process that causes copper from an underlying metallization layer 10 to be redeposited on the sidewalls of the vias 16 (page 5, line 35 through page 6, line 6; Fig 2).

According to the present invention, the above copper contamination problem is solved by forming a first diffusion barrier layer 111 (Fig. 3J) on and contacting a first metallization layer 110 and forming a second etch stop layer 113 on and contacting the first diffusion barrier layer 111, as recited in independent claim 4. A first etch stop layer 112 is then formed on and

contacting the second etch stop layer 113, and a dielectric layer 114 is formed on and contacting the first etch stop layer 112. After etching the dielectric layer 114 and the first etch stop layer 112, the second etch stop layer 113 and the first diffusion barrier layer 111 are left unetched (page 10, lines 16-18, Fig. 3F). During reverse sputtering of the second etch stop layer 113 and the first diffusion barrier layer 111, material from the first diffusion barrier layer 111 is redeposited on the sidewalls of the via 116 to form a sidewall diffusion barrier layer 119 (page 10, lines 22-25), which prevents subsequent copper contamination caused by reverse sputtering of the metallization layer 110 (page 10, lines 25-28). The present invention, thus, constitutes an improvement over conventional semiconductor devices by providing a multi-layer stack of etch stop layers and a diffusion barrier layer that are used to protect against copper contamination.

VI. ISSUES

The Issues Which Arise In This Appeal And Require Resolution By The Honorable Board of Patent Appeals And Interferences (The Board) Are:

1. Whether claim 4 is unpatentable under 35 U.S.C. § 102 for lack of novelty based upon Zhou et al., U.S. Patent No. 6,475,810 (hereinafter Zhou).; and
2. Whether claim 3 is unpatentable under 35 U.S.C. § 103 for obviousness based upon Zhou in view of Li et al., U.S. Patent No. 6,331,479 (hereinafter Li).

VII. GROUPING OF CLAIMS

The appealed claims do not stand or fall together as a group. Independent claim 4 stands or falls alone, and dependent claim 3 stands or falls alone.

VIII. THE ARGUMENT

THE REJECTION OF CLAIM 4 UNDER 35 U.S.C. § 102 FOR LACK OF NOVELTY BASED UPON ZHOU

In the statement of the rejection the Examiner referred to Fig. 3B of Zhou and identified certain features in Zhou that allegedly correspond to features recited in claim 4. The following chart identifies the claim feature in column 1, the reference numeral in Zhou referred to by the Examiner in disclosing this feature in column 2, and how Zhou characterizes the feature identified by this same reference numeral in column 3.

Features in claim 4	Alleged disclosing Ref #	Description of Ref# in Zhou
(i) a first metallization layer	14	lower interconnect 14 (column 2, line 42); metallic layer of copper 14 (column 4, line 29)
(ii) a first diffusion barrier layer disposed on and contacting said first metallization layer	16	embedded organic stop layer 16 ... preferably a low-k material (column 2, lines 47-65)
(iii) a second etch stop layer disposed on and contacting said first diffusion layer	18	passivation layer 18 (column 3, lines 1-7)
(iv) a first etch stop layer disposed on and contacting said second etch stop layer	20	dielectric layer 20 (column 3, lines 8-15)
(v) a dielectric layer disposed on and contacting said first etch stop layer	22*	optional etch stop layer 22 (column 3, lines 23-26)
(vi) a via extending through said dielectric layer, said first etch stop layer, said second etch stop layer and said first diffusion barrier layer	32	via opening 32 (column 3, line 47)
(vii) wherein said second etch stop layer has a thickness of at least 50 angstroms to about 120 angstroms	see column 3, lines 4-5	"The passivation layer 18 preferably has thickness of between about 50 and 1,000Å."

* In a telephone interview, the Examiner asserted that reference numeral 22 was incorrectly designated as reference numeral 24 in the Office Action dated December 1, 2003. As shown in Fig. 3B of Zhou, layer 24 of Zhou does not contact the alleged first etch stop layer 20. Thus, feature 24 of Zhou could not identically disclose feature (v). Although Zhou does mention that layer 22 is optional, which would place layer 24 in contact with layer 22, Zhou also states that layer 24 is formed from the same materials as layer 20. Thus, layer 20 could not act as an etch stop if it is formed from the same material as layer 24.

The factual determination of anticipation under 35 U.S.C. § 102 requires the identical disclosure of each element of a claimed invention in a single reference. As part of this analysis, the Examiner must (a) identify the elements of the claims, (b) determine the meaning of the elements in light of the specification and prosecution history, and (c) identify corresponding elements disclosed in the allegedly anticipating reference. The Examiner, however, has failed to establish that Zhou identically disclose each element of the claimed invention. In this regard, Appellants refer to features (ii), (iv) and (v) of claim 4 identified above.

Notwithstanding that the Examiner has identified certain features in Zhou that the Examiner asserts corresponds to features (ii), (iv) and (v) of claim 4, Appellants respectfully submit that the Examiner's analysis was based upon improper constructions for the meanings of these claim terms. Specifically, the Examiner has not given any weight to the terms "diffusion barrier," "etch stop," and "dielectric" as these terms are used to modify the term "layer." Instead, the Examiner has taken the position that any of the layers disclosed by Zhou is capable of functioning as a diffusion barrier layer, etch stop layer, or dielectric layer.

By way of example, reference is made to the Office Action dated December 18, 2002, in which claim 4 was previously rejected under 35 U.S.C. § 102 based upon Zhou. In that Office Action, the Examiner asserted that feature 22 disclosed the claimed first diffusion barrier layer, whereas in the present Office Action, the Examiner asserted that feature 22 disclosed the claimed dielectric layer. The Examiner also asserted that feature 16 disclosed the claimed second etch stop layer, whereas in the present Office Action, the Examiner asserted that feature 16 disclosed the claimed first diffusion barrier layer. As such, depending upon the particulars of Appellants' claims, the Examiner appears to be adjusting the interpretation of the claim language so as to justify the rejection.

Each term in a claim should be given its ordinary and customary definition such that when the prior art is viewed in light of the knowledge of one skilled in the art, a determination can be made as to whether or not the particular feature was disclosed by the prior art. Appellants submit that the Examiner has not given the terms in claim 4 their ordinary and customary definition and not interpreted the prior art in view of these definitions. As alluded to above, the Examiner's interpretation of the terms in the claims do not, for example, distinguish between a layer and a diffusion barrier layer or a layer and an etch stop layer.

Given the broadest possible interpretation of the term "diffusion barrier layer," any layer, even a layer of air, can act as a barrier to diffusion, and thus all layers could conceivably be considered a diffusion barrier layer. Such an interpretation, however, would fail to give any meaning to the term "diffusion barrier" in the context of the claimed invention. However, claims

are to be given their ordinary and customary meaning accorded to them by those skilled in the art in the context of the claimed invention. Since a diffusion barrier layer is commonly recognized in the semiconductor art as a particular type of layer having a particular function, Appellants respectfully submit that not all layers would be recognized as diffusion barrier layers by those skilled in this particular art. In applying this analysis to the present situation, there is no factual basis that supports a finding that one skilled in the art would recognize that the organic stop layer 16 of Zhou is a diffusion barrier layer, as that term is customarily used.

Similarly, in the broadest sense of the term "etch stop layer," any metal or non-metallic layer could conceivably act as an etch stop. However, as discussed above, the issue as to whether or not a particular claimed feature is disclosed by the prior art must be resolved by determining the ordinary and customary meaning of the claimed feature as understood by one skilled in the art (i.e., would one having ordinary skill in the art recognize that the claimed feature is disclosed by the applied prior art). In the Final Office Action, the Examiner asserted that feature 20 of Zhou corresponded to the claimed etch stop layer and feature 22 corresponded to the claimed dielectric layer. Zhou, however, states the exact opposite in describing feature 22 as an etch stop layer and feature 20 as a dielectric layer. On the basis that Zhou distinguished a dielectric layer from an etch stop layer and Zhou can be considered as "one skilled in the art," Appellants submit that Zhou has already determined that feature 22 is an etch stop layer and feature 20 is a dielectric layer and, hence, not an etch stop layer. Thus, there is no factual basis that supports a finding that one skilled in the art would recognize that the dielectric layer 20 of Zhou corresponds to the claimed etch stop layer or that the etch stop layer 22 of Zhou corresponds to the claimed dielectric layer.

The above argued failures of Zhou to identically disclose each element of the claimed invention undermines the Examiner's determination that Zhou describes the claimed invention within the meaning of 35 U.S.C. § 102. Appellants, therefore, respectfully submit that the imposed rejection of claim 4 under 35 U.S.C. § 102 for anticipation based upon Zhou is not factually viable.

THE REJECTION OF CLAIM 3 UNDER 35 U.S.C. § 103 FOR OBVIOUSNESS BASED UPON ZHOU IN VIEW OF LI

On page three of the Final Office Action, the Examiner asserted that one having ordinary skill in the art would have been motivated to modify Zhou to replace the silicon carbide and silicon oxynitride of the claimed second etch stop layer with silicon oxide "because silicon carbide, silicon oxynitride and silicon oxide are commonly used as the etch stop layer and they are interchangeable," as allegedly taught by Li.

Claim 3 depends ultimately from independent claim 4, and Appellants incorporate herein the arguments previously advanced in traversing the imposed rejection of claim 4 under 35 U.S.C. § 102 for anticipation based upon Zhou. Furthermore, the secondary reference to Li does not cure the argued deficiencies of Zhou. Accordingly, the proposed combination of references would not yield the claimed invention. Notwithstanding these arguments, one having ordinary skill in the art would not have been motivated to modify Zhou in view of Li.

Feature 20 in Zhou (i.e., the alleged first etch stop layer) is described as silicon oxide (column 3, lines 11-14). As claimed, the first etch stop layer is formed on and contacting the

second etch stop layer, and thus, the second etch stop layer acts to stop the etching process after the first etch stop layer has been etched. However, if feature 18 of Zhou (i.e., the alleged second etch stop layer) is modified to be formed from silicon oxide, as suggested by the Examiner, then how could a silicon oxide feature (i.e., feature 18) act to stop the etching of a silicon oxide feature 20? An etch stop layer operates by having a greater etch resistance than the material being etched to the etchant being used. However, since both features are formed from silicon oxide, there is no reason to believe that one silicon oxide layer would have a greater resistance to a particular etchant than the other silicon oxide layer. Thus, one having ordinary skill in the art would not have been motivated to modify the alleged second etch stop layer of Zhou in view of Li because to do so would negate the ability of the second etch stop layer to act as an etch stop layer.

IX. CONCLUSION

It should, therefore, be apparent that the Examiner has failed to establish, within the meaning of 35 U.S.C. § 102, that Zhou teaches all of the claimed limitations found in claim 4. Furthermore, one having ordinary skill in the art would not have been motivated to modify Zhou in view of Li to arrive at the limitations recited in claim 3.

X. PRAYER FOR RELIEF

Based upon the foregoing, Appellants respectfully submit that one having ordinary skill in the art would not have found the claimed invention identically disclosed by Zhou or that one having ordinary skill in the art would have found the claimed invention obvious based upon Zhou in view of Li. Appellants, therefore, respectfully solicit the Honorable Board to reverse the

Application No.: 09/785,445

Examiner's rejections under 35 U.S.C §§ 102, 103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

A handwritten signature in black ink, appearing to read 'Scott D. Paul', is written over the firm name.

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APPENDIX

3. The semiconductor device according to claim 4, wherein said second etch stop layer includes silicon oxide.

4. A semiconductor device, comprising:

- a first metallization layer;
- a first diffusion barrier layer disposed on and contacting said first metallization layer;
- a second etch stop layer disposed on and contacting said first diffusion layer;
- a first etch stop layer disposed on and contacting said second etch stop layer;
- a dielectric layer disposed on and contacting said first etch stop layer;
- a via extending through said dielectric layer, said first etch stop layer, said second etch stop layer and said first diffusion barrier layer, wherein said second etch stop layer has a thickness of at least 50 angstroms to about 120 angstroms.